AMENDMENTS TO THE SPECIFICATION

On page 6, please replace the paragraph covering lines 10-15 within the amended paragraph, as follows:

Fig. 22 shows typical timing charts of operations carried out by the CDR circuit shown in Fig. 19. As a method of further reducing the clock control interval, there is a method in which a dual counter is employed for carrying out process A and process B concurrently. Of course, there is also a method of using a ~~sigle~~ single counter for processing process A only.

On page 8, please replace the first paragraph, beginning on line 1, thereof, with the amended paragraph, as follows:

With clock timing 1, the phase of the clock signal is compared with the phase of data by comparing the rising edge of the clock signal with the rising edge of a data pulse far way from an eye. In the case of clock timing 1, the falling edge of the clock signal is shifted to a position outside the eye serving as a data recovery width, existing in the 0.7 UI jitter range. Thus, if the fact that data jitters deviate from D0 to Dn is taken into consideration, at Dn, for example, it is quite within the bounds of possibility that the data preceding Dn by 1 cycle is output. With clock timing 2, on the other hand, the phase of the clock signal is compared with the phase of data by comparing the rising edge of the clock signal with the rising edge of a data pulse close to the eye serving as ~~an eye~~ a data recovery width. Also in the case of clock timing 2, the falling edge of the clock signal is shifted to a position outside the eye serving as a data recovery width, existing in the 0.7 UI jitter range. Thus, if the fact that data jitters deviate from D0 to Dn is taken into consideration, at D0, for example,

it is quite within the bounds of possibility that the data succeeding D0 by 1 cycle is output.